



## DATA SHEET

# MOS INTEGRATED CIRCUIT

## $\mu$ PD3573

### 2 048-BIT CCD LINEAR IMAGE SENSOR

The  $\mu$ PD3573 is a 2 048-bit linear image sensor consisting of charge coupled devices (CCDs), which converts light to voltage. This product is made up of a 2 048-bit photosensor array, charge transfer register with a pair of 1 024-bit CCDs, and sample and hold circuit. The photosensor has a 14  $\mu$ m pitch.

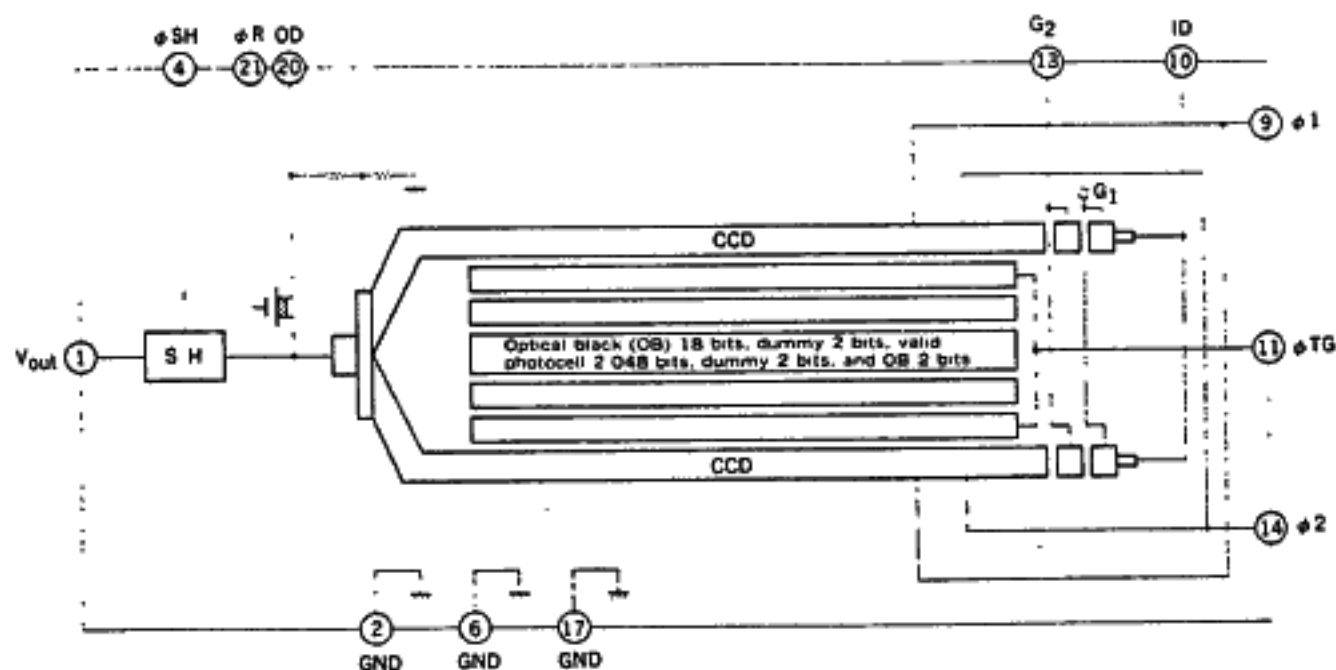
#### FEATURES

- Incorporates a sample and hold circuit.
- High response sensitivity: Providing a response ten times better than the existing equivalent NEC product ( $\mu$ PD799D) to the light from a white fluorescent lamp
- Peak response wavelength: 550 nm green
- Reads the shorter side of a B4-size sheet at a resolution of 8 dot/mm
- Driven by a 12 V single power supply

#### ORDERING INFORMATION

| Part Number   | Package                               |
|---------------|---------------------------------------|
| $\mu$ PD3573D | 22-pin ceramic DIP (CERDIP) (400 mil) |

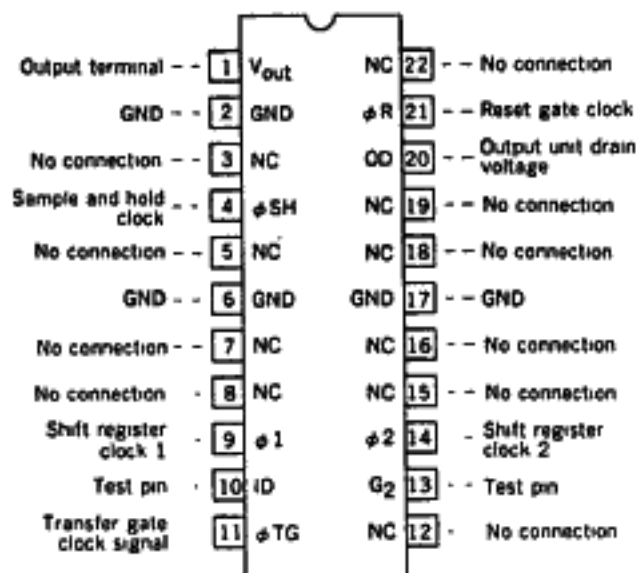
#### BLOCK DIAGRAM



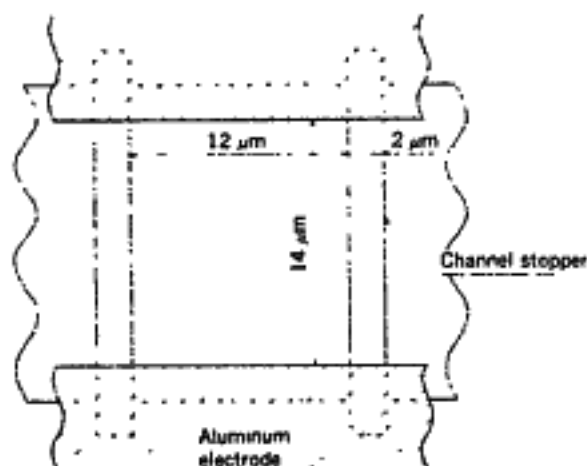
NEC cannot assume any responsibility for any circuits shown or represent that they are free from patent infringement.

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## PIN CONNECTION DIAGRAM (Top View)



## PHOTOELEMENT STRUCTURE DIAGRAM

ABSOLUTE MAXIMUM RATINGS ( $T_a = 25^\circ C$ )

|                                     |               |             |            |
|-------------------------------------|---------------|-------------|------------|
| Output unit drain voltage           | $V_{OD}$      | -0.3 to +15 | V          |
| Test pin $I_D$ voltage              | $V_{ID}$      | -0.3 to +15 | V          |
| Shift register clock signal voltage | $V_{\phi 1}$  | -0.3 to +15 | V          |
|                                     | $V_{\phi 2}$  | -0.3 to +15 | V          |
| Reset signal voltage                | $V_{\phi R}$  | -0.3 to +15 | V          |
| Transfer gate signal voltage        | $V_{\phi TG}$ | -0.3 to +15 | V          |
| Sample and hold signal voltage      | $V_{\phi SH}$ | -0.3 to +15 | V          |
| Operating ambient temperature       | $T_{op1}$     | -25 to +60  | $^\circ C$ |
| Storage temperature                 | $T_{stg}$     | -40 to +100 | $^\circ C$ |

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RECOMMENDED OPERATING CONDITIONS ( $T_a = -25$  to  $+60^\circ\text{C}$ )

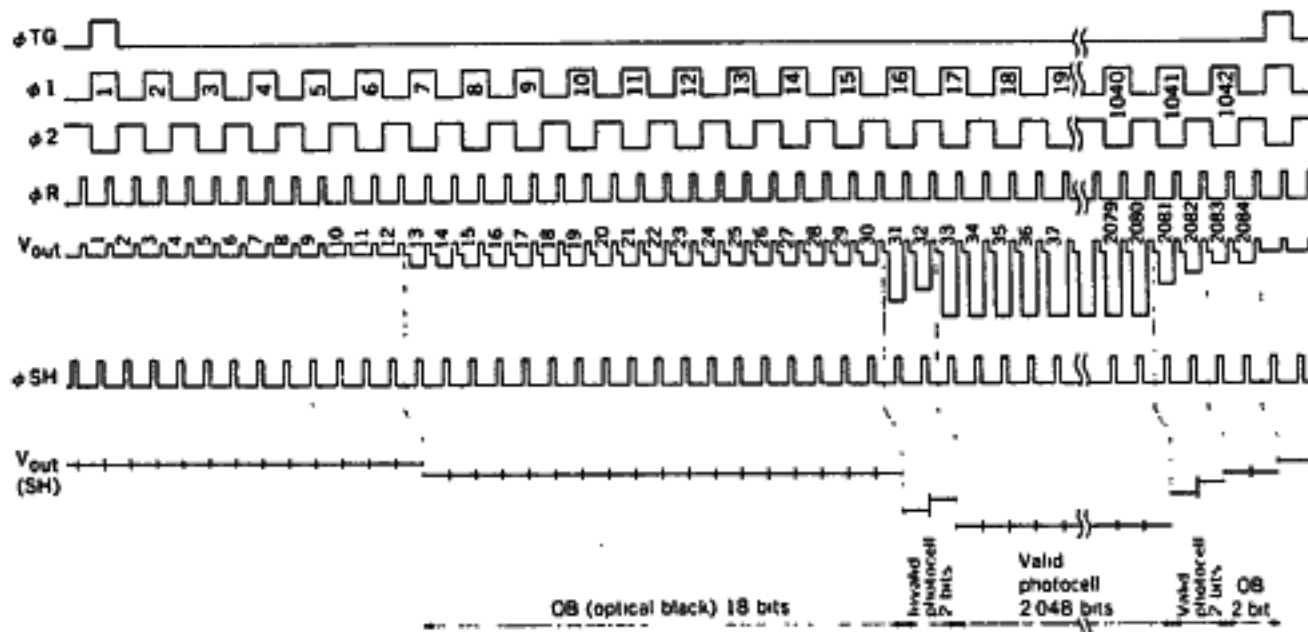
| ITEM                                     | SYMBOL         | MIN. | TYP. | MAX. | UNIT |
|------------------------------------------|----------------|------|------|------|------|
| Output unit drain voltage                | $V_{OD}$       | 11.4 | 12.0 | 12.6 | V    |
| Test pin $G_2$ voltage                   | $V_{G2}$       |      | 0    |      | V    |
| Test pin ID voltage                      | $V_{ID}$       |      | 12.0 |      | V    |
| Shift register clock 1 signal high level | $V_{\phi 1H}$  | 4.5  | 5.0  | 12.6 | V    |
| Shift register clock 1 signal low level  | $V_{\phi 1L}$  | -0.3 | 0    | 0.5  | V    |
| Shift register clock 2 signal high level | $V_{\phi 2H}$  | 4.5  | 5.0  | 12.6 | V    |
| Shift register clock 2 signal low level  | $V_{\phi 2L}$  | -0.3 | 0    | 0.5  | V    |
| Reset signal RH high level               | $V_{\phi RH}$  | 8.0  | 12.0 | 12.6 | V    |
| Reset signal RL low level                | $V_{\phi RL}$  | -0.3 | 0    | 1.0  | V    |
| Transfer gate signal high level          | $V_{\phi TGH}$ | 4.5  | 5.0  | 12.6 | V    |
| Transfer gate signal low level           | $V_{\phi TGL}$ | -0.3 | 0    | 0.5  | V    |
| Sample and hold signal high level        | $V_{\phi SHH}$ | 8.0  | 12.0 | 12.6 | V    |
| Sample and hold signal low level         | $V_{\phi SHL}$ | -0.3 | 0    | 1.0  | V    |
| Data rate                                | $f_{\phi R}$   |      | 1    | 3    | MHz  |

ELECTRICAL CHARACTERISTICS ( $T_a = 25^\circ\text{C}$ ,  $V_{OD} = 12.0\text{ V}$ ,  $f_{\phi 1} = 1\text{ MHz}$ , data rate = 2 MHz, storage time = 10 ms, light source: 2 856 K tungsten bulb.)

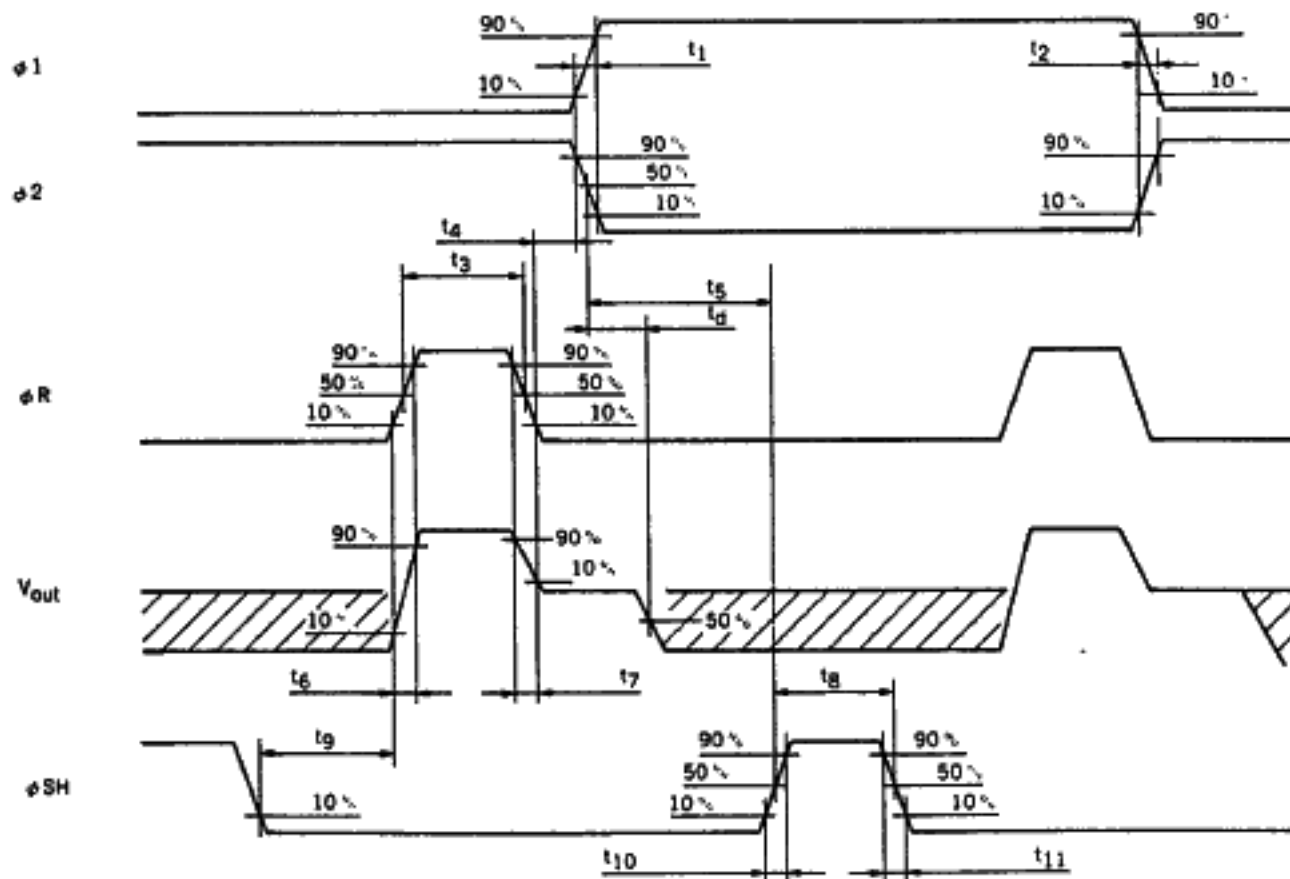
| ITEM                                       | SYMBOL        | MIN. | TYP.    | MAX.     | UNIT       | TEST CONDITIONS                            |
|--------------------------------------------|---------------|------|---------|----------|------------|--------------------------------------------|
| Saturation voltage                         | $V_{sat}$     | 1.4  | 2.0     |          | V          |                                            |
| Saturation exposure                        | SE            |      | 0.3     |          | Lxs        | White fluorescent lamp                     |
| Photo response non-uniformity              | PRNU          |      | $\pm 5$ | $\pm 10$ | %          | $V_{out}$ : 500 mV, white fluorescent lamp |
| Average dark signal                        | ADS           |      | 1       | 5        | mV         | Optical input interruption                 |
| Dark signal non-uniformity                 | DSNU          |      | 3       | 10       | mV         | Optical input interruption, peak value     |
| Power consumption                          | $P_w$         |      | 50      | 100      | mW         |                                            |
| Output impedance                           | $Z_o$         | 0.3  | 0.6     | 1        | k $\Omega$ |                                            |
| Response                                   | R             | 12.6 | 18.0    | 23.4     | V/Lxs      | W lamp                                     |
|                                            | R             | 4.2  | 6.0     | 7.8      | V/Lsk      | White fluorescent lamp                     |
| Response peak wavelength                   |               |      | 550     |          | nm         |                                            |
| Offset level                               | $V_{OS}$      | 4.5  | 6.5     | 8.5      | V          |                                            |
| Input capacity of shift register clock pin | $C_{\phi 1}$  |      | 700     | 1000     | pF         |                                            |
|                                            | $C_{\phi 2}$  |      |         |          |            |                                            |
| Reset pin input capacity                   | $C_{\phi R}$  |      | 5       | 15       | pF         |                                            |
| Input capacity of sample and hold pin      | $C_{\phi SH}$ |      | 5       | 15       | pF         |                                            |
| Input capacity of transfer gate signal pin | $C_{\phi TG}$ |      | 50      | 150      | pF         |                                            |
| Output rise delay time                     | $t_d$         |      | 20      | 50       | ns         |                                            |

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## TIMING CHART

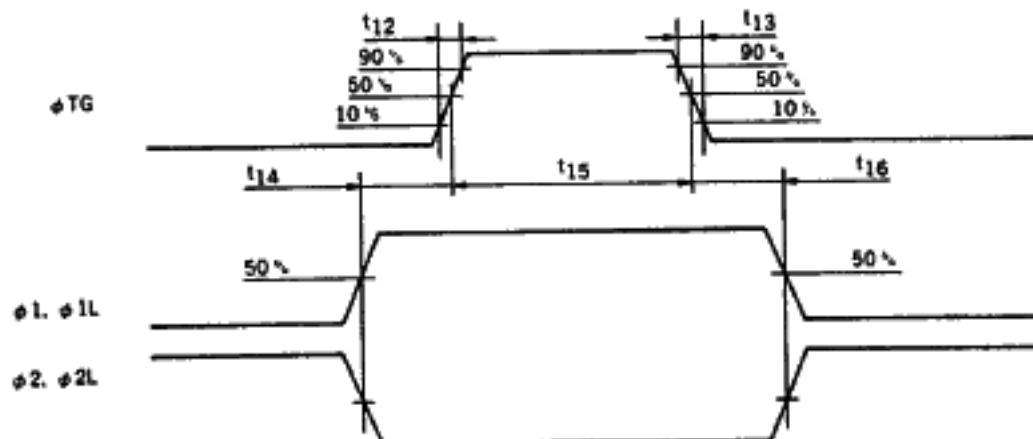


Note:  $V_{out}$  = Output when SH not used  
 $V_{out}(SH)$  = Output when SH used

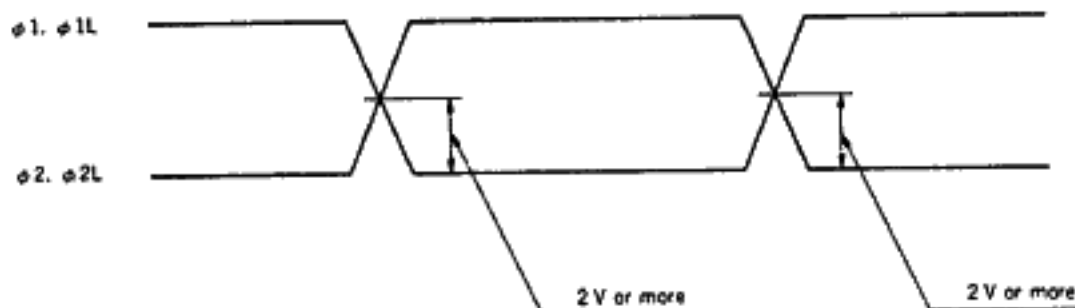
Timing chart for  $\phi 1$ ,  $\phi 2$ ,  $\phi R$ ,  $\phi SH$ , and  $V_{out}$ 

Timing chart for  $\phi TG$ ,  $\phi 1$ ,  $\phi 1L$ ,  $\phi 2$ ,  $\phi 2L$

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Cross points  $\phi 1$ ,  $\phi 1L$ ,  $\phi 2$ ,  $\phi 2L$



| Name             | MIN. | TYP. | MAX. |
|------------------|------|------|------|
| $t_1, t_2$       | 0    | 50   | 150  |
| $t_3$            | 20   | 250  |      |
| $t_4$            | 0    | 20   | 500  |
| $t_5$            | 100  | 200  | 500  |
| $t_6, t_7$       | 0    | 20   | 50   |
| $t_8$            | 50   | 100  |      |
| $t_9$            | 0    | 20   |      |
| $t_{10}, t_{11}$ | 0    | 20   | 100  |
| $t_{12}, t_{13}$ | 0    | 50   | 100  |
| $t_{14}, t_{16}$ | 10   | 100  |      |
| $t_{15}$         | 300  | 1000 |      |

(ns)

## DEFINITIONS OF CHARACTERISTIC ITEMS

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1. Saturation voltage:  $V_{sat}$

The point at which the response linearity is lost.

2. Saturation exposure: SE

Product of intensity of illumination (lx) and storage time (s) when saturation of output voltage occurs

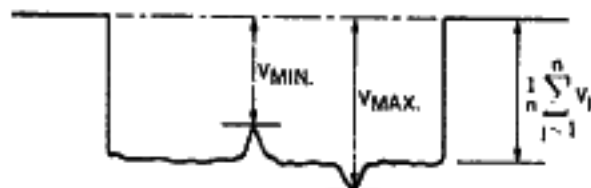
3. Photo response non-uniformity: PRNU

Expressed by the following expressing with the peak/bottom ratio to the average output voltage of all the valid bits.

$$PRNU(\%) = \left( \frac{V_{MAX. \text{ or } V_{MIN.}}}{\frac{1}{n} \sum_{j=1}^n V_j} - 1 \right) \times 100$$

$n$  : Number of valid bits

$V_j$  : Output voltage of each bit



4. Average dark signal: ADS

Output average voltage in light shielding

$$ADS(mV) = \frac{1}{n} \sum_{j=1}^n V_j$$

5. Dark signal non-uniformity: DSNU

Peak output voltage to the idle level in light shielding



6. Output impedance:  $Z_o$

Output pin impedance when viewed externally

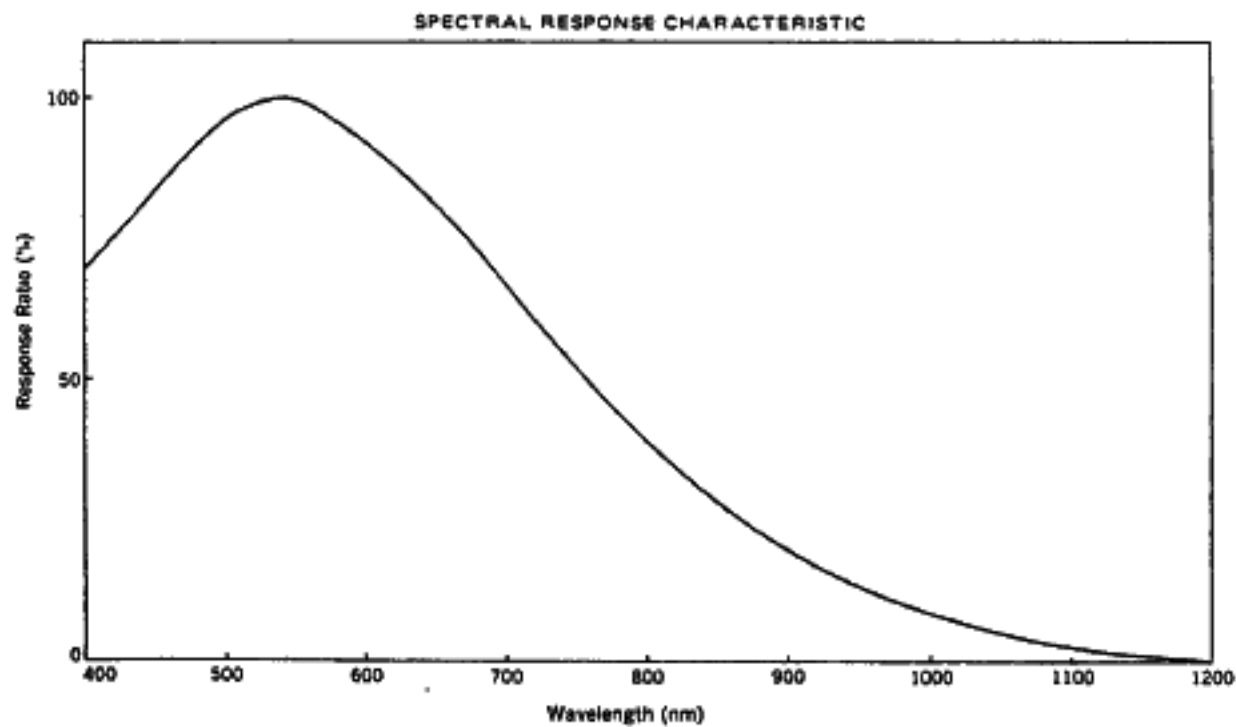
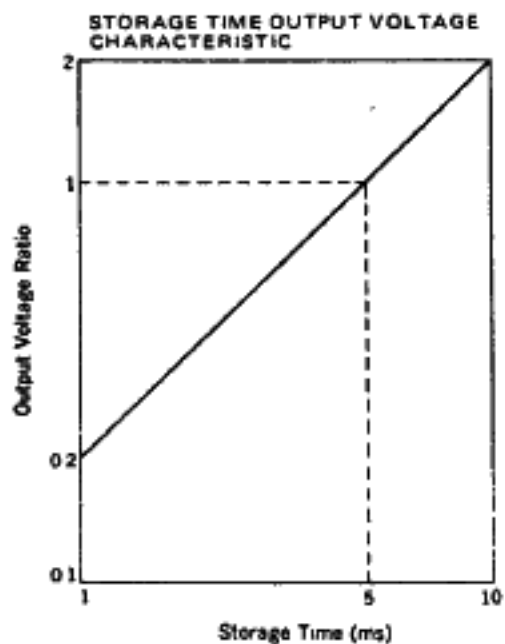
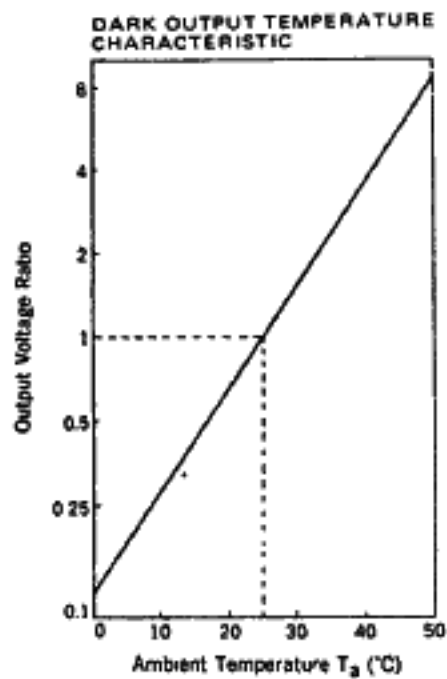
7. Response: R

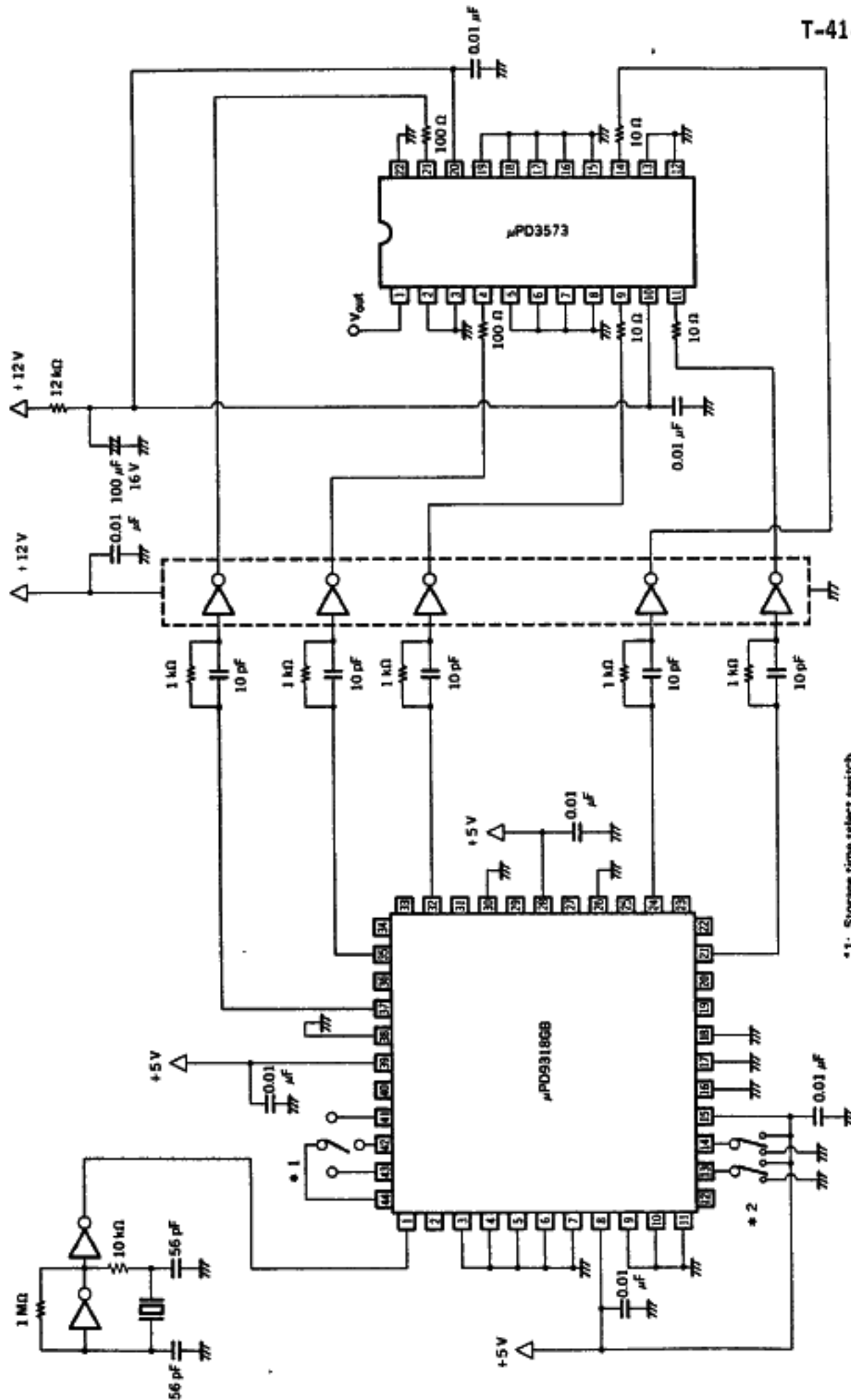
Output voltage divided by exposure (lx-s).

Note that the response varies with the light source.

JARD CHARACTERISTIC CURVES ( $T_a = 25^\circ\text{C}$ )

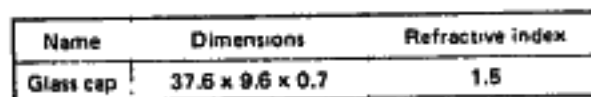
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### PACKAGE DIMENSIONS (Unit: mm)



**Note:** For a reference board, use this package in open status without applying electric potential.